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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,854	10/29/2003	Hsin-Fu Tseng	586	9748

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EXAMINER	
SOHN, SEUNG C	
ART UNIT	PAPER NUMBER
2878	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,854	TSENG ET AL.	
	Examiner	Art Unit	
	SEUNG C. SOHN	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet **within the range of 50 to 150 words**. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Fossum et al. (Patent No. US 5,665,959).

Regarding claim 1, Fossum et al. shows in Fig. 3 an inverter (-A1), at least one photodiode detector (PD) serving as a scanning light sensing element, an integration capacitor (Cin), an AC coupling mechanism, and video output means (Vout) comprising at least one output source follower circuit; wherein said inverter is a low-power, high-

gain, single-stage inverter that serves as an integration amplifier to clamp said light sensing element at a fixed bias voltage, said integration capacitor has a capacitance value that is much smaller than an effective capacitance of said photodiode detector, said integration capacitor being used to provide a pixel gain, and said AC coupling mechanism stores and cancels reset noise of said integration capacitor, thereby allowing the implementation of a high sensitivity sensor with minimum noise (Col. 7, lines 34-48).

Regarding claim 2, Fossum et al. shows in Fig. 3 that said capacitance value of said integration capacitor is at least ten times smaller than said effective capacitance of said photodiode detector.

Regarding claim 3, Fossum et al. shows in Fig. 3 that said circuit further comprises a cross-bar output structure to cancel an offset voltage of each pixel introduced by a threshold variation of a pair of said output source follower circuits.

Regarding claim 4, Fossum et al. shows in Fig. 3 that: said photodiode detector is an n-p junction photodiode.

Regarding claim 5, Fossum et al. shows in Fig. 3 that said photodiode detector is a p-n junction photodiode.

Regarding claim 6, Fossum et al. shows in Fig. 4 that said inverter (-A1) comprises at least two transistors and at least one bias voltage, one of said transistors functions as a current source, and remaining ones of said transistors (Q1, Q2 or Q3) are cascode transistors to increase gain and to isolate input and output nodes (Col. 7, line 63 – Col. 8, line .

Regarding claim 7, Fossum et al. shows in Fig. 3 that a loading capacitor is used to reduce a frequency bandwidth of said inverter to reduce a thermal noise level.

Regarding claim 8, Fossum et al. shows in Fig. 3 that said video output means comprises a cross-bar circuit including at least three transistors to reset hold capacitors of said scanning circuit and to eliminate a dark offset of each pixel.

Regarding claim 9, Fossum et al. shows in Fig. 3 that each pixel circuit of said scanning circuit receives input from two detectors, thereby providing a lowered resolution array with higher sensitivity and lower scanning time.

Regarding claim 10, Fossum et al. shows in Fig. 3 that said scanning light sensing element is an interdigitated array structure comprising at least two linear arrays, said linear arrays being offset by one half pixel in an array direction and one line distance in a scanning direction, each said linear array having one half a desired resolution, said linear arrays being paired to achieve said desired resolution, thereby providing higher sensitivity and lower cost.

Regarding claim 11, Fossum et al. shows in Fig. 3 that said linear arrays share output processing circuits, including a digital scanning register, IS and IR current sources, OS and OR common video lines, and follow-on differential amplifier stages, thereby providing smaller sensor chip size, lower power dissipation, and higher scanning speed.

Regarding claim 12, Fossum et al. shows in Fig. 3 that each pixel circuit of said scanning circuit receives input from at least two detectors, thereby providing a lowered resolution array with higher sensitivity and lower scanning time.

Regarding claim 13, Fossum et al. shows in Fig. 3 that said scanning light sensing element comprises at least two linear arrays, each of said linear arrays being selectively disabled to provide multiple resolution settings for said scanning circuit.

Regarding claim 14, Fossum et al. shows in Fig. 3 an inverter (-A1), at least one photodiode detector (PD) serving as a scanning light sensing element, an integration capacitor (Cin), an AC coupling mechanism, and video output means (Vout) comprising at least one output source follower circuit; wherein said scanning light sensing element is an interdigitated array structure comprising at least two linear arrays, said linear arrays being offset by one half pixel in an array direction and one line distance in a scanning direction, each said linear array having one half a desired resolution, said linear arrays being paired to achieve said desired resolution, thereby providing higher sensitivity and lower cost.

Regarding claim 15, Fossum et al. shows in Fig. 3 that said linear arrays share output processing circuits, including a digital scanning register, IS and IR current sources, OS and OR common video lines, and follow-on differential amplifier stages, thereby providing smaller sensor chip size, lower power dissipation, and higher scanning speed.

Regarding claim 16, Fossum et al. shows in Fig. 3 that each pixel circuit of said scanning circuit receives input from at least two detectors, thereby providing a lowered resolution array with higher sensitivity and lower scanning time.

Regarding claim 17, Fossum et al. shows in Fig. 3 that said scanning light sensing element comprises at least two linear arrays, each of said linear arrays being selectively disabled to provide multiple resolution settings for said scanning circuit.

Regarding claim 18, Fossum et al. shows in Fig. 3 that said inverter is a low-power, high-gain, single-stage inverter that serves as an integration amplifier to clamp said light sensing element at a fixed bias voltage, said integration capacitor has a capacitance value that is much smaller than an effective capacitance of said photodiode detector, said integration capacitor being used to provide a pixel gain, and said AC coupling mechanism stores and cancels reset noise of said integration capacitor, thereby allowing the implementation of a high sensitivity sensor with minimum noise.

Regarding claim 19, Fossum et al. shows in Fig. 3 that said capacitance value of said integration capacitor is at least ten times smaller than said effective capacitance of said photodiode detector.

Regarding claim 20, Fossum et al. shows in Fig. 3 that said circuit further comprises a cross-bar output structure to cancel an offset voltage of each pixel introduced by a threshold variation of a pair of said output source follower circuits.

Regarding claim 21, Fossum et al. shows in Fig. 3 that said photodiode detector is an n-p junction photodiode.

Regarding claim 22, Fossum et al. shows in Fig. 3 that said photodiode detector is a p-n junction photodiode.

Regarding claim 23, Fossum et al. shows in Fig. 3 that said inverter comprises at least two transistors and at least one bias voltage, one of said transistors functions as

a current source, and remaining ones of said transistors are cascode transistors to increase gain and to isolate input and output nodes.

Regarding claim 24, Fossum et al. shows in Fig. 3 that a loading capacitor is used to reduce a frequency bandwidth of said inverter to reduce a thermal noise level.

Regarding claim 25, Fossum et al. shows in Fig. 3 that said video output means comprises a cross-bar circuit including at least three transistors to reset hold capacitors of said scanning circuit and to eliminate a dark offset of each pixel.

Regarding claim 26, Fossum et al. shows in Fig. 7 an interdigitated array structure comprising at least two linear arrays (12), said linear arrays being offset by one half pixel in an array direction and one line distance in a scanning direction, each said linear array having one half a desired resolution, said linear arrays being paired to achieve said desired resolution, thereby providing higher sensitivity and lower cost.

Regarding claim 27, Fossum et al. shows in Fig. 3 that said linear arrays share output processing circuits, including a digital scanning register, IS and IR current sources, OS and OR common video lines, and follow-on differential amplifier stages, thereby providing smaller sensor chip size, lower power dissipation, and higher scanning speed.

Regarding claim 28, Fossum et al. shows in Fig. 3 that each pixel circuit of said scanning circuit receives input from at least two detectors, thereby providing a lowered resolution array with higher sensitivity and lower scanning time.

Regarding claim 29, Fossum et al. shows in Fig. 3 that said scanning light sensing element comprises at least two linear arrays, each of said linear arrays being selectively disabled to provide multiple resolution settings for said scanning circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SEUNG C. SOHN whose telephone number is (571)272-4123. The examiner can normally be reached on Mon-Thur, 7:30 AM -6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, GEORGIA Y. EPPS can be reached on 571-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SEUNG C SOHN/

Examiner, Art Unit 2878